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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,240	04/23/2004	Girish A. MADPUWAR	TI-36330	3239

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,240	MADPUWAR ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered June 16, 2006.

- Claims 1-19 are pending.
- Claim 7 is amended.

Response to Amendment

Applicant's arguments and amendments with respect to amended claim 7 and previously presented claims 1-6 & 8-19 filed June 16, 2006 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, that Nadeau-Dostie et al. fails to teach or suggest a first enable signal which is synchronized with the first clock. The Examiner respectfully disagrees.

Nadeau-Dostie al. teaches "Primary controller 210 operates under the control of a main test clock signal, BistClk, outputs test vectors at output PRPG to a corresponding input in the auxiliary test controller, and receives the responses to applied test vectors at an MISR input from an output of the auxiliary test controller, outputs a clock enable signal CEE, a configuration control signal SE[3] and a **scan enable** signal, SE, which would be applied to memory elements in **synchronous clock domains** if they had been shown in the figure." (Figure 7, colum 30, lines 15-40) Therefor, clearly a first scan enable signal is being generated, which is synchronous to the clock domain as taught in claim 1.

Specification

The Applicant recites "totesting" (paragraph [0002]). The Applicant is required to correct it to to testing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 6-9, 11, and 13 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Nadeau-Dostie et al. US Pat no. 6442722 B1.

As per claim 1:

Nadeau-Dostie et al. teaches a method of generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique (column 3, lines 15-50), wherein said sequential scanning technique is designed to operate said integrated circuit in a scan mode if said accurate scan enable signal is at a first logic level (column 3, lines 60-67) and in a capture mode if said accurate scan enable signal is at a second logic level (column 4, lines 1-10), said method comprising: receiving a first scan enable signal having a first transition from said first logic level to said second logic level (Figure 4, "ScanEnableHS", column 6, lines 30-33) and a second transition from said second logic level to said first logic level (column 6, lines 38-41); and generating said accurate scan enable signal from said first scan enable signal by timing said first transition to be synchronous with a clock signal (column 6, lines 30-33), and

passing said second transition on said accurate scan enable signal asynchronously (column 6, lines 38-41).

As per claim 2:

Nadeau-Dostie et al. teaches the method as rejected in claim 1, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit (Figure 5 # 120, 122, 124, 126, column 12, lines 14-19), said clock signal containing a plurality of low speed clock pulses in which a scan sequence is scanned into said plurality of memory elements in said scan mode (Figure 4, # 130, column 12, lines 15-65), said clock signal further containing a plurality of high speed clock pulses in which said integrated circuit is operated in said capture mode (Figure 4, # 132, column 12, lines 15-65).

As per claim 3:

Nadeau-Dostie et al. teaches the method as rejected in claim 2, wherein said first scan enable signal is received from a test equipment (Figure 5 # 50), wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse (Figure 4, "SE"), and said second transition is received after said plurality of high speed clock pulses (Figure 4, "ScanEnableHS") wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses (Figure 4).

As per claim 4:

Nadeau-Dostie et al. teaches a presettable circuit generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique (column 3, lines 15-50), wherein said sequential scanning technique is designed to

operate said integrated circuit in a scan mode if said accurate scan enable signal is at a first logic level (column 3, lines 60-67) and in a capture mode if said accurate scan enable signal is at a second logic level (column 4, lines 1-10), said presettable circuit comprises: a flip-flop containing a preset input and an output (Figure 2 # 84, column 6, lines 10-12), wherein said preset input is coupled to receive a first scan enable signal and said output is coupled to provide said accurate scan enable signal (column 7, lines 12-24), whereby said accurate scan enable signal transitions to said first logic level asynchronously (column 6, lines 38-41).

As per claim 5:

Nadeau-Dostie et al. teaches the presettable circuit as rejected in claim 4, said flip-flop further contains a data input (Figure 2, "D") and a clock input (Figure 2, "CK"), wherein said data input and said clock input receive said first scan enable signal and a clock signal respectively (column 7, lines 12-24), whereby said accurate scan enable signal transitions to said second logic level synchronously (column 6, lines 30-33).

As per claim 6:

Nadeau-Dostie et al. teaches the presettable circuit as rejected in claim 5, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit (Figure 5 # 120, 122, 124, 126, column 12, lines 14-19), said clock signal containing a plurality of low speed clock pulses in which a scan sequence is scanned into said plurality of memory elements in said scan mode (Figure 4, # 130, column 12, lines 15-65), said clock signal further containing a plurality of high speed

clock pulses in which said integrated circuit is operated in said capture mode (Figure 4, # 132, column 12, lines 15-65).

As per claim 7:

Nadeau-Dostie et al. teaches the presettable circuit as rejected in claim 5, wherein said first scan enable signal is received from a test equipment (Figure 5 # 50), wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse (Figure 4, "SE"), and said second transition is received after said plurality of high speed clock pulses (Figure 4, "ScanEnableHS") wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses (Figure 4).

As per claim 8:

Nadeau-Dostie et al. teaches the presettable circuit as rejected in claim 5, wherein said flip-flop comprises a D flip-flop (Figure 2 # 84, column 6, lines 10-12).

As per claim 9:

Nadeau-Dostie et al. teaches a gating circuit generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique (column 3, lines 15-50), wherein said sequential scanning technique is designed to operate said integrated circuit in a scan mode if said accurate scan enable signal is at a first logic level (column 3, lines 60-67) and in a capture mode if said accurate scan enable signal is at a second logic level (column 4, lines 1-10), said gating circuit comprises: a flip-flop receiving a first scan enable signal as an input and being clocked by a clock signal (Figure 2 # 84, column 6, lines 10-12), whereby transitions on an output of said flip-flop

are synchronous with said clock signal (column 6, lines 30-33); and a logic gate receiving said first scan enable signal as a first input (Figure 2 # 74) and said output of said flip-flop as another input (column 9, lines 1-10), said logic gate generating said accurate scan enable signal as said output (figure 2, "SEHS"), said logic gate passing said first logic level received on said first scan enable signal to said output such that said accurate scan enable signal transitions asynchronously to said first logic level (column 9, lines 5-60), and whereby transitions to said second logic level are synchronous with said clock signal (column 6, lines 30-33).

As per claim 10:

Nadeau-Dostie et al. teaches the gating circuit rejected in claim 9, wherein said logic gate comprises an OR gate (column 9, lines 1-10).

As per claim 11:

Nadeau-Dostie et al. teaches the gating circuit as rejected in claim 11, wherein said flip-flop comprises a D flip-flop (Figure 2 # 84, column 6, lines 10-12).

As per claim 12:

Nadeau-Dostie et al. teaches the gating circuit as rejected in claim 9, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit (Figure 5 # 120, 122, 124, 126, column 12, lines 14-19), said clock signal containing a plurality of low speed clock pulses in which a scan sequence is scanned into said plurality of memory elements in said scan mode (Figure 4, # 130, column 12, lines 15-65), said clock signal further containing a plurality of high speed

clock pulses in which said integrated circuit is operated in said capture mode (Figure 4, # 132, column 12, lines 15-65).

As per claim 13:

Nadeau-Dostie et al. teaches the gating circuit as rejected in claim 11, wherein said first scan enable signal is received from a test equipment (Figure 5 # 50), wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse (Figure 4, "SE"), and said second transition is received after said plurality of high speed clock pulses (Figure 4, "ScanEnableHS") wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses (Figure 4).

As per claim 14:

Nadeau-Dostie et al. teaches an apparatus generating an accurate scan enable signal when testing an integrated circuit using a sequential scanning technique (column 3, lines 15-50), wherein said sequential scanning technique is designed to operate said integrated circuit in a scan mode if said accurate scan enable signal is at a first logic level (column 3, lines 60-67) and in a capture mode if said accurate scan enable signal is at a second logic level (column 4, lines 1-10), said apparatus comprising: means for receiving a first scan enable signal having a first transition from said first logic level to said second logic level (Figure 4, "ScanEnableHS", column 6, lines 30-33) and a second transition from said second logic level to said first logic level (column 6, lines 38-41); and means for generating said accurate scan enable signal from said first scan enable signal by timing said first transition to be synchronous with a clock signal (column 6,

lines 30-33), and passing said second transition on said accurate scan enable signal asynchronously (column 6, lines 38-41).

As per claim 15:

Nadeau-Dostie et al. teaches the apparatus as rejected in claim 14, wherein said clock signal is used to clock a plurality of memory elements contained in said integrated circuit (Figure 5 # 120, 122, 124, 126, column 12, lines 14-19), said clock signal containing a plurality of low speed clock pulses in which a scan sequence is scanned into said plurality of memory elements in said scan mode (Figure 4, # 130, column 12, lines 15-65), said clock signal further containing a plurality of high speed clock pulses in which said integrated circuit is operated in said capture mode (Figure 4, # 132, column 12, lines 15-65).

As per claim 16:

Nadeau-Dostie et al. teaches the apparatus as rejected in claim 15, wherein said first scan enable signal is received from a test equipment (Figure 5 # 50), wherein said first transition of said first scan enable signal is received before a rising edge of a first high speed clock pulse (Figure 4, "SE"), and said second transition is received after said plurality of high speed clock pulses (Figure 4, "ScanEnableHS") wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses (Figure 4).

As per claim 17:

Nadeau-Dostie et al. teaches an integrated circuit comprising: a combinational logic generating a plurality of outputs based on a plurality of inputs column 2, lines 29-65); a plurality of memory elements connected in sequence and being clocked by a

clock signal (columns 2-3, lines 29-55), each of said plurality of memory elements operable in a scan mode or a capture mode according to an accurate scan enable signal (Figure 4, column 6, lines 30-41), wherein a scan sequence is scanned into said plurality of memory elements as said plurality of inputs in said scan mode and said plurality of outputs are captured in said capture mode (column 6, lines 14-51); and a generation circuit receiving a first scan enable signal containing a first transition from said scan mode to said capture mode and a second transition from said capture mode to said scan mode (Figure 2 # 96), said generation circuit generating said accurate scan enable signal with said first transition being timed to be synchronous (column 6, lines 30-33) with said clock signal and with said second transition being asynchronous (column 6, lines 38-41).

As per claim 18:

Nadeau-Dostie et al. teaches the integrated circuit as rejected in claim 17, wherein said clock signal contains a plurality of low speed clock pulses and a plurality of high speed clock pulses (Figure 4), wherein said integrated circuit is operated in said capture mode in a time duration corresponding to said high speed clock pulses (Figure 4, # 132, column 12, lines 15-65) and in said scan mode in a time duration corresponding to said low speed clock pulses(Figure 4, # 130, column 12, lines 15-65).

As per claim 19:

Nadeau-Dostie et al. teaches the integrated circuit as rejected in claim 18, wherein said first scan enable signal is received from a test equipment (Figure 5 # 50), wherein said first transition of said first scan enable signal is received before a rising

edge of a first high speed clock pulse (Figure 4, "SE"), and said second transition is received after said plurality of high speed clock pulses (Figure 4, "ScanEnableHS") wherein said first high speed clock pulse is contained in said plurality of high speed clock pulses (Figure 4).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to the final action is set to expire in THREE MONTH from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part

of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
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07/30/2006

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